Combinatorial Tools for Materials Science

Combinatorial materials science has rapidly become a new paradigm for the acceleration of materials research. It is a fast and efficient methodology for materials optimization and discovery, characterized by high throughput, parallel experiments, automated analysis, and massive data sets. NIST's industrial stakeholders are identifying it as the only viable technique for understanding complex materials science systems in a competitive timeframe. Its application to a critical materials science problem in the Si microelectronics industry, the replacement of the gate stack, is expected to drive an inorganic combinatorial materials science program at NIST.

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NIST/MSEL is poised to play several important roles in developing combinatorial materials methodologies, especially as they pertain to industrially important, advanced inorganic materials. Included in this class are materials such as thermoelectrics, dielectric and metal layers for advanced Si CMOS gate stacks, multiferroics, magnetic semiconductors for spintronics, transparent semiconductors, and fuel cell and H_2 storage materials. NIST/MSEL has an opportunity to take a lead position in the use of combinatorial methodologies for:

- New, combinatorially-friendly (rapid, local, microscopic measurements) metrologies;
- Materials optimization and development;
- Means of experimentally verifying computed materials properties;
- Tools for determining phase diagrams and other property data; and
- "Data on demand," or "just-in-time-data."

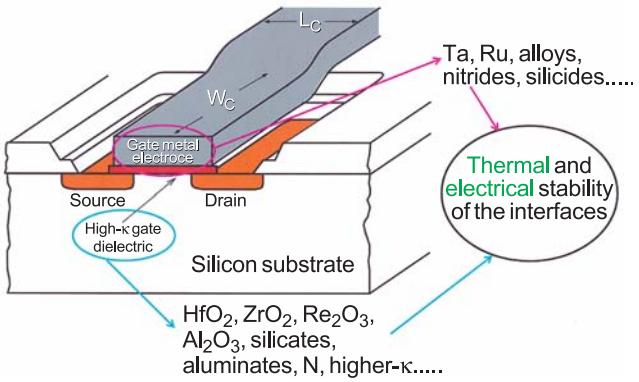

Figure 1: *MOSFET device with advanced gate stack.*

The advanced gate stack application for Si CMOS is a good example. International Sematech (ISMT) is currently faced with major materials challenges to further miniaturization. Figure 1 schematically illustrates a metal oxide-semiconductor field effect transistor (MOSFET), showing the advanced gate stack which consists of the high-κ (κ = dielectric constant) gate dielectric and the metal gate electrode. To enable further device scaling, the capacitive equivalent thickness (CET) of the gate stack thickness must be 0.5 nm to 1.0 nm. This will not be achievable with existing SiO_2/polycrystalline Si gate stacks. Given the large number of possible choices for these new layers, the only feasible approach to understanding the complex materials interactions that result at the gate dielectric/substrate and gate dielectric/metal gate electrode interfaces is through the application of combinatorial methodologies.

The acquisition of a state-of-the-art combinatorial synthesis tool is expected be one of the cornerstones of the NIST/MSEL effort. In addition, we plan to acquire combinatorially-friendly tools such as a micro-x-ray diffractometer, and to develop new metrologies such as nanocalorimetry for the detection of phase transformations in thin films.

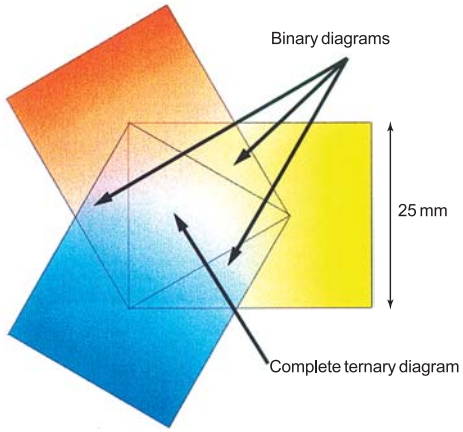

Figure 2: *Combinatorial ternary and binary film libraries.*

The new combinatorial synthesis tool will be capable of depositing entire ternary and binary libraries in areas as small as 6.5 cm^2 (1 in^2), as is shown in Figure 2.

Contributors and Collaborators

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